REMARKS

The above-referenced application has been reviewed in light of the Examiner's Office Action dated January 14, 2004. Nonelected Claims 17-20 have been canceled. Accordingly, Claims 1-16 are currently pending in this application, and no new matter has been added. The Examiner's reconsideration of the rejections in view of the above amendments and the following remarks is respectfully requested.

In accordance with the Office Action, the Examiner has maintained the restriction requirement and required cancellation of the nonelected claims. Accordingly, Claims 17-20 have been canceled.

In accordance with the Office Action, Claims 12-16 stand rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. The Applicant respectfully traverses. The Examiner has indicated that "nowhere does the Applicant teach 'correcting erasures and then actual errors in the code words using the erasure flags'." O.A. at 3. The Examiner's attention is drawn to the Application, page 15, lines 19-23, for example, which teaches that "The ... decoder ... determines the information data symbols ... associated with the first erasure flag ... . After the erasure correction is performed on the erasure symbols, the error correction is performed on the ... data symbols ...". Accordingly, the Applicant does teach "correcting erasures and then actual errors in the code words using the erasure flags."

The Examiner has also cited Applicant's "Brief Description of the Drawings" (App. at 8, lines 1-2) to conclude no teaching of erasure correction prior to error correction. It is submitted that the necessarily brief description of Figure 6, or of any other figure in

the "Brief Description of the Drawings", is merely introductory and not limiting. For example, "a method for channel decoding and error correcting" may also be "for" other purposes, such as correcting erasures, for example, without transgressing the introductory brief description. Although Figure 6 represents one possible embodiment of the presently claimed invention, the actual implementation of the function blocks (e.g., 640 and 655) must be read in conjunction with the entire written description, including, for example, the case processes described prior to Figure 6 (*see, e.g.,* App. at 15, *supra.*). Therefore, Figure 6 does not preclude "correcting erasures and then actual errors in the code words using the erasure flags," as taught in the Application (*Id.*). Accordingly, Claims 12-16 do comply with the written description requirement of 35 U.S.C. §112, first paragraph.

In accordance with the Office Action, Claims 1-11 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that Applicant regards as the invention. The Applicant respectfully traverses. The Examiner has indicated that the term 'error-erasure correction' has an accepted meaning as "...an error correction means using information about erased locations to correct errors." In Applicant's Response to the prior Office Action, Applicant's use in the Application and Claims of the term 'error-erasure correction' was summarized to "include the decoding step of quickly determining if there are any erasures so that they may be more efficiently corrected prior to performing any attempted correction of actual errors for which error locations are unknown." The Application was originally written in a foreign language and translated into English.

During preparation of the prior Response, the translated Application was carefully reviewed by the undersigned with the resulting summarization of the term 'error-erasure correction'. The Examiner is correct that the term 'quickly' may be relative. The word 'quickly' may be read as and/or replaced with the word 'first'. However, this shortcoming is non-fatal to Applicant's summarized meaning since the meaning is instructive even if the term 'quickly' is merely omitted.

The Examiner's citation of 'efficiently coded' as relative may be out of context. In the prior Response, 'error-erasure correction' was summarized for the Examiner to "include the decoding step of ... determining if there are any erasures so that they may be more efficiently corrected prior to performing any attempted correction of actual errors for which error locations are unknown." Thus, the plain meaning of this summary sets forth that erasures may be "more efficiently corrected" if determined "prior to ... correction of actual errors." The amount 'more' is not important since it is not a step but a result. What may be important is any improvement over the prior art accomplished by Applicant's teachings.

It is clear from the Application in its entirety that Applicant has developed a correction process capable of correcting erasures and then actual errors (*see, e.g.,* Application, page 15, lines 19-23, *supra.*). The fact that the phrase that Applicant chose to refer to this process translated from a foreign language into 'error-erasure correction' must not be allowed to detract from Applicant's teachings themselves. In addition, the Examiner's recitation of an accepted meaning in the art as "...an error correction means using information about erased locations to correct errors" is not incongruent with

Applicant's usage, since Applicant also teaches "...using information about erased locations to correct errors" by first determining erasures (locations known) to facilitate subsequent correction of errors (locations unknown). Accordingly, Claims 1-11 are not indefinite per 35 U.S.C. §112, second paragraph.

In accordance with the Office Action, Claims 12-16 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that Applicant regards as the invention. The Applicant respectfully traverses. The Examiner has asserted that "erasures are actual errors" (O.A. at 5). Equation 1, as introduced and described in the Background section of the Application (App. at 2, lines 12-23), clearly differentiates erasures from actual errors. Locations of erasures are known, while locations of actual errors are unknown. *See also,* App. at 16, lines 13-14. Therefore, the recitation in Claim 12 of "correcting erasures and then actual errors in the code words using the erasure flags" is not indefinite. In addition, the Application sets forth that erasure flags are used directly for correcting erasures (*see* App. at 10, lines 9-13), and that embodiments may also use erasure information in conjunction with other information for correcting actual errors (*see* App. at 12, lines 15-23). Thus, it is clear from Claim 12, when read in conjunction with the Application as a whole, that the erasure flags are used for correcting erasures, and that they may also be used for correcting actual errors. Accordingly, Claims 12-16 are not indefinite per 35 U.S.C. §112, second paragraph.

In accordance with the Office Action, Claims 1-3 and 5-7 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,112,324 to Howe et al. (the

'324 patent). Applicants' respectfully submit with traverse that Claims 1 and 5, and those depending therefrom, are not anticipated by the '324 patent for at least the reasons set forth below.

The '324 patent to Howe, et al., is directed to a system for redefining the data *distribution* for a compact disc ("CD") to provide a direct access storage device ("DASD") while using "a conventional CIRC encoder/decoder" (Howe at Abstract, line 14). Consequently, Howe focuses on sector headers and physical distribution of data on a CD rather than on decoding of the data itself.

To summarize a CD embodiment of the present invention, an EFM demodulator receives channel code symbols and demodulates each valid channel code symbol to an information data symbol. For each invalid channel code symbol, the EFM demodulator provides an arbitrary information data symbol or one that is also an erasure symbol, and further sets a first single-bit erasure flag for each invalid channel code symbol. The information data symbols and corresponding first erasure flags are sent to a buffer.

The buffer assembles a C1 word including information data symbols and their corresponding first erasure flags, and provides this C1 word to a C1 decoder. The novel C1 data decoder of the present invention begins by checking for erasures using the first single-bit erasure flags of the current C1 word, which may be efficiently OR'ed together, as will be readily understood by those skilled in the art for such single-bit flags, to quickly determine if there are any erasures. If there are any erasures in the current C1 word, the C1 decoder proceeds to correct a correctable number of erasures. The C1 decoder then corrects a correctable number of actual errors, where the correctable

number of actual errors is dependent upon the number of erasures, that is, it is reduced by one correctable actual error for every two erasures corrected.

If, on the other hand, there are no first erasure flags set for the current C1 word, only then does the C1 decoder of the present invention proceed along more conventional lines to correct only actual errors of the current C1 word. If the number of erasures and/or actual errors is too great for the C1 decoder to handle, this C1 decoder sets each information data symbol of the current C1 word to an arbitrary information data symbol or one that is also an erasure symbol, and further sets a second erasure flag for each symbol of the current C1 word. The information data symbols and their corresponding second erasure flags are provided to the buffer.

The buffer uses the symbols and second erasure flags provided by the C1 decoder to assemble a C2 word including information data symbols and their corresponding second erasure flags, and provides the C2 word to a C2 decoder. The C2 decoder of the present invention begins by correcting a correctable number of erasures, and then corrects a correctable number of actual errors, where the correctable number of actual errors is dependent upon the number of erasures. If the number of erasures and/or actual errors is too great for the C2 decoder to handle, this C2 decoder sets each information data symbol of the current C2 word to an arbitrary information data symbol or one that is also an erasure symbol. The information data symbols are provided to the buffer.

Applicants' pending Claim 1 recites, *inter alia*,

"(b) producing demodulated data including the information data symbols and erasure flags by demodulating the channel data symbols, using the channel code; and

(c) performing error-erasure correction on the information data symbols produced in the step (b), using error locations indicated by the erasure flags having a predetermined value..."

It is well established in the field of patent law that an applicant is his/her own lexicographer. Applicants have used the phrase "error-erasure correction" to include the decoding step of determining if there are any erasures (with known locations) prior to performing correction of any actual errors (with unknown locations). This usage is more specific, but not incongruent, with other usage of the term in the art. Howe, on the other hand, clearly admits to using "a conventional CIRC encoder/decoder", and therefore neither teaches nor suggests the use of a modified encoder. In addition, Howe actually teaches away from the use of a modified decoder by reciting motivation to remain with a conventional decoder to maintain compatibility with the then-current standards (*See, e.g.,* Howe at Abstract, lines 11-14; col. 4, lines 38-43; col. 5, lines 13-23; col. 8, lines 27-31).

The Examiner's reliance on Howe at col. 8, lines 42-51 is misplaced. It is not disputed that some prior art marked some information data symbols as erasures and/or "deleted" them prior to actual error correction. Embodiments of the present invention flag *and correct* such erasures of information data symbols with the first decoder (e.g., C1 or PI) prior to correcting any actual errors. Nowhere does Howe teach or suggest *the correction* of erasures prior to correction of actual errors, and particularly not

correction of erasures *with the first or same decoder* to be subsequently used for correction of actual errors. Thus, Howe merely follows the prior art by treating demodulated symbol erasures as actual errors when performing a first *actual error correction using a conventional C1 decoder.*

Likewise, the Examiner's citation to Howe at col. 8, lines 60-64 merely confirms that Howe's C1 decoder "performs error correction", as opposed to the more efficient error-erasure correction (erasures corrected before actual errors) of Applicants' present disclosure and claims.

The Examiner's citation to Howe at col. 15, lines 10-17, merely describes special synchronization characters chosen by Howe to synchronize sector headers in a direct access device, or DASD. Since these synchronization codes apply only to sector headers rather than to data, as known in the art, these synchronization codes do not constitute information data symbols, *as colorably admitted by Howe* (Howe at col. 15, lines 12-14).

The citation to Howe at col. 16, lines 13-16, has been taken out of context. This entire paragraph, beginning at col. 15, line 51, is directed to describing "sector ID fields in header frames" (Howe, col. 15, line 51). The specific requirements of Howe's sector/header frames are incongruent with those of regular data, and apparently require extra-careful decoding at considerable expense to ensure synchronization. Howe recognized that the treatment of regular data would have to remain "conventional" due to the relatively inefficient nature of Howe's either/or erasure/error correction for synchronization headers.

Thus, it is to the credit of the present Applicants that a greater benefit can now be provided (i.e., erasure *and* error correction at *each* decoder) with a reduced processing overhead (e.g., single-bit OR'able erasure flags) as compared to the prior art and Howe.

Similarly, Applicants' pending Claim 5 recites, *inter alia*,

"a channel decoder ... for producing demodulated data having the information data symbols and erasure flags by demodulating the channel data symbols, using the channel code.

a memory for storing the demodulated data outputted from the channel decoder; and

a decoding unit for performing an error-erasure correction on the information data symbols, using error locations indicated by the erasure flags having a predetermined value..."

Thus, Applicants' recitation of the above features, particularly the "decoding unit for performing an error-erasure correction on the information data symbols...", also render the pending Claim 5 novel over Howe.

Accordingly, Applicants' pending independent Claims 1 and 5 are neither anticipated nor rendered obvious by the '324 patent to Howe et al. Each of Claims 2-3 and 6-7 ultimately depends from one of independent Claims 1 or 5, and necessarily includes each of the elements and limitations thereof. Therefore, each of Claims 1-3 and 5-7 is not anticipated or rendered obvious by Howe et al., nor by any of the other references of record in this case.

In accordance with the Office Action, Claims 4, 8 and 12-13 stand rejected under 35 U.S.C. §103(a) as being obvious over U.S. Patent No. 6,112,324 to Howe et al. (the '324 patent). Applicants' respectfully submit with traverse that Claims 4 and 8 are not rendered obvious by the '324 patent for at least the reasons set forth below, and respectfully submit without traverse that previously amended Claims 12-13 are not rendered obvious by the '324 patent for at least the reasons set forth below.

The remarks given above to refute anticipation of Claims 1-3 and 5-7 are similarly applicable here to refute obviousness of Claims 4, 8 and 12-13 in view of the same Howe reference.

The Examiner has also cited Howe at col. 27, lines 36-40, to support the contention that Howe taught the use of a single-nibble erasure flag to indicate a double-nibble erasure. It is respectfully submitted that using a 4-bit "flag" to indicate an 8-bit erasure is substantially less efficient than using a 1-bit flag to mark the symbol location of an 8-bit information data symbol erasure. Such a scheme is certainly less efficient than that recited in Applicants' pending dependent Claim 4, for example.

In addition, the 4-bit "flag" of Howe is not used for the same purpose as the 1-bit first erasure flag of Applicants' present disclosure, which is to use a first decoder to perform erasure correction, where applicable, prior to using the same decoder to perform actual error correction.

Thus, Claim 4 is neither taught nor suggested by Howe, et al. Claim 8 recites language similar to Claim 4 and is not rendered obvious for the same reasons.

Claim 12, which does not recite the coined error-erasure term, has been previously amended to recite, *inter alia*,

"correcting erasures and then actual errors in the code words using the erasure flags."

Howe neither teaches nor suggests correcting erasures prior to actual errors. Therefore, previously amended Claim 12 is not rendered obvious by Howe, et al. Claim 13 depends from Claim 12, and is likewise not rendered obvious.

In accordance with the Office Action, Claims 9-11 and 14-16 stand rejected under 35 U.S.C. §103(a) as being obvious over U.S. Patent No. 6,112,324 to Howe et al. (the '324 patent) in view of U.S. Patent No. 5,392,299A to Rhines et al. (the '299 patent). Applicants' respectfully submit with traverse that Claims 9-11 and 14-16 are not rendered obvious by Howe in view of Rhines for at least the reasons set forth below.

Claims 9-11 depend from independent Claim 5, and are not rendered obvious by Howe for the same reasons that Claim 5 is not rendered obvious by Howe, as discussed above. Claims 14-16 depend from independent Claim 12, and are not rendered obvious by Howe for the same reasons that Claim 12 is not rendered obvious by Howe, as discussed above. Rhines, which is directed to a complex triple-orthogonality error correction system, fails to cure the above-described deficiencies of Howe with respect to Applicants' presently claimed invention. In addition, the added computational complexity of Rhines teaches away from a motivation for Applicants' present invention, which was to achieve more efficient error correction in higher speed environments. Thus, one of ordinary skill in the pertinent art would not be motivated to

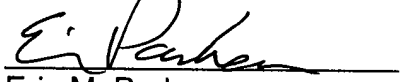
combine the teachings of Howe with the teachings of Rhines, and even if they did, would not arrive at Applicants' presently claimed invention.

Therefore, each of Claims 1-16 are neither anticipated nor rendered obvious by the '324 patent to Howe et al., whether taken alone or in combination with any of the other references of record in this case.

Conclusion

Accordingly, it is respectfully submitted that independent Claims 1, 5 and 12 are in condition for allowance for at least the reasons stated above. Since Claims 2-4, 6-11 and 13-16 each depend from one of the above claims and necessarily include each of the elements and limitations thereof, it is respectfully submitted that these claims are also in condition for allowance for at least the reasons stated, and for reciting additional patentable subject matter. Thus, each of Claims 1-16 is in condition for allowance. All issues raised by the Examiner having been addressed, reconsideration of the rejections and an early and favorable allowance of this case is earnestly solicited.

Respectfully submitted,

By: 

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